An L-Band, LTCC Frequency Doubler Using Embedded Lumped Element Filters

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Abstract - **We have demonstrated an L-Band frequency doubler (1.5 GHZ, 33% BW) using an LTCC (Low Temperature Co-fired Ceramic) substrate. Lumped element filters were embedded in an LTCC carrier, providing greater than 10:1 footprint reduction over a previous single-layer hybrid implementation.**

I. Introduction

Sandia National Laboratories has demonstrated high resolution airborne synthetic aperture radar (SAR) for several years [1]-[2]. Passive frequency doublers are used in the SAR to both expand and upconvert a linear FM chirp to the proper operational frequency and bandwidth. Current frequency doubler stages are implemented using hybrid technology with commercially available components on single-layer, aluminum-backed Rodgers 6002 Duroid.

Size reduction is desirable when extending SAR applications to such platforms as UAVs (Unmanned Ariel Vehicles) and satellites. The footprint of a single layer hybrid stage is large since all circuitry must exist side-by-side on the same layer. One method of footprint reduction would be to embed filters [3] within the internal structure of a multi-layer carrier fabricated with LTCC technology. Below is a size comparison of the hybrid technology and proposed LTCC implementation for a low frequency multiplier stage:

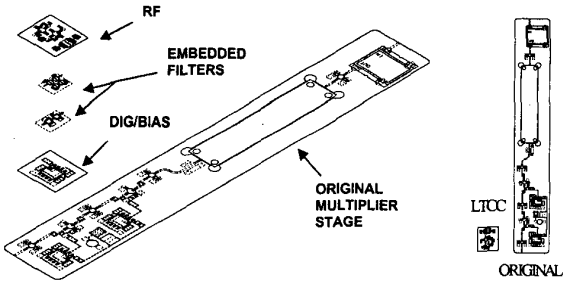

Fig 1. Size Reduction of Low Frequency Doubler

With the filters embedded, the surface of the substrate would be available for surface mount components such as frequency doublers, mixers or bias circuitry. Design of embedded filters would require robust design, extensive simulation and process-tolerant architecture. To ensure the feasibility of this approach, a frequency doubler test circuit was designed, fabricated and characterized.

II. Filter Design

The proposed doubler stage schematic is shown below:

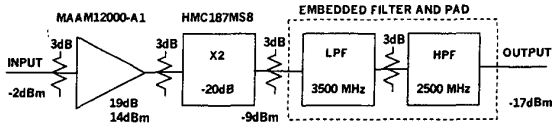

Fig 2. Frequency Doubler Chain

To avoid radar sidelobe degradation, unwanted energy at the fundamental and 3rd harmonic frequencies at the doubler output should be reduced to a minimum of 40 dB below the desired signal at the 2nd harmonic. The commercial doubler (from Hitite) is expected to produce levels of 15 dBc and 26 dBc at the fundamental and 3rd harmonic, respectively, when operated at the drive level provided by the MA/COM gain block.

The embedded high pass/low pass filter combination must then supply at least 25 dB of rejection from 1250-1750 MHz and 14 dB of rejection from 3750-5250 MHz. Padding is provided to ensure a good match between components. The third attenuator is a surface mount device from EMC, compatible with Thermopad technology, to provide gain adjustment over temperature if required. Other attenuators are fixed values consisting of printed pi resistor networks.

Lumped element filters were designed to meet the above specifications using the Ferro A6 tape system (ε_r=5.9, height=7.4 mils). An elliptic filter with parallel L-C resonators was chosen for the low pass design. The layout and approximate equivalent circuit are shown below.

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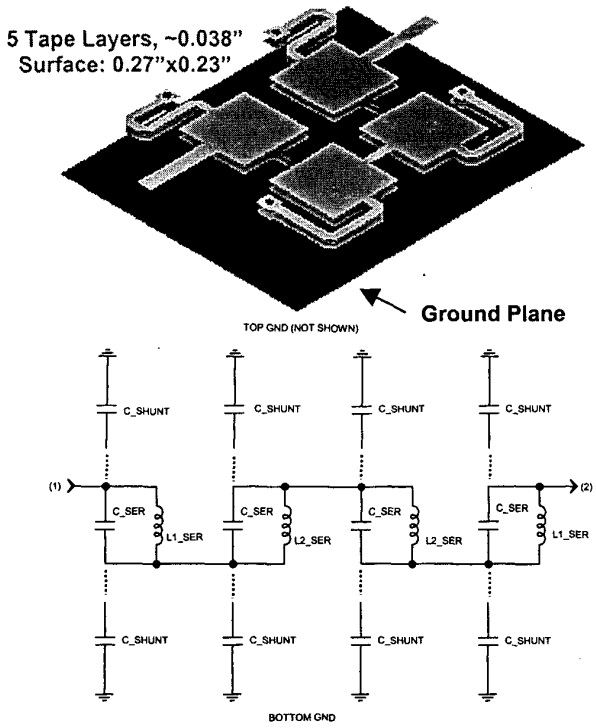

Fig 3. LPF Layout and Equivalent Circuit

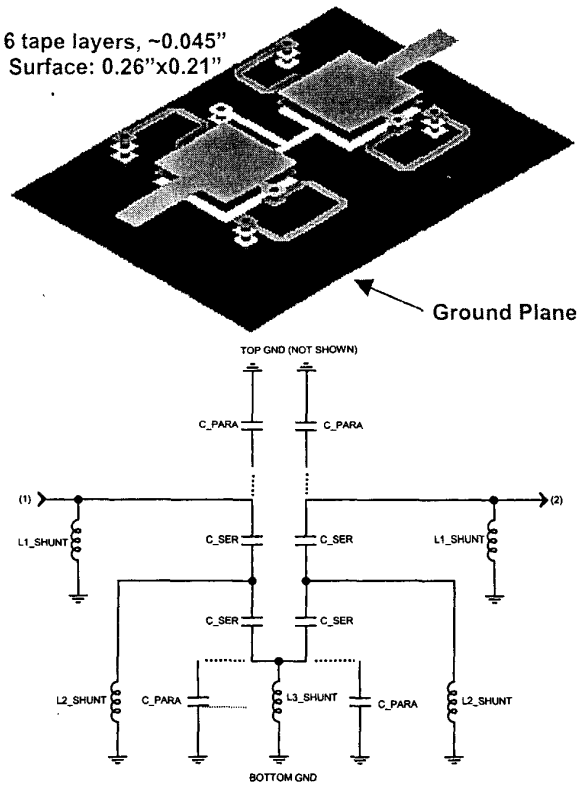

Fig 4. HPF Layout and Equivalent Circuit

Preliminary values for the elliptic filter elements were derived using the =FILTER= synthesis module in the Eagleware GENESYS circuit simulator. The series capacitance is formed by placing parallel plates between a single layer of tape. Since the circuit has shielded ground plane both above and below the conductors, the shunt capacitance will also be related to the size of the plate used to form the series capacitors. Forcing the shunt capacitance to an integer value of the series capacitance at internal nodes allows some capacitance adjustment by addition of tape layers between the plate and ground.

Initial values from =FILTER= suggest the total shunt capacitance (2*C_SHUNT) at internal circuit nodes needs to be about equal to the series capacitance value, or that the shunt capacitance of a single plate should be half of the series capacitance value. In this design, two layers where needed between the series plates and ground to provide the appropriate capacitance ratio. The series inductors (the narrow lines with the via) were then tuned for the attenuation curve at the band of interest.

The geometry and topology of the all-pole high pass filter is shown below:

Series capacitance values were forced to be equal in the topology so that a stack of identically sized plates could be used. This both reduces the foot print of the filter (at the expense of increased number of layers) and eliminates the need to interconnect series capacitors with small transmission line sections that could introduce unwanted series inductance and degrade filter performance. Shunt inductors were again realized as thin transmission lines to ground and were used to optimize the filter response over the band of interest.

Unlike the low pass filter, shunt capacitance to ground is not part of the desired topology and appears as an unwanted parasitic in this design. To reduce shunt capacitance, two dielectric layers were added above and below the capacitor stack (voids above and below the series capacitor plates in either design could have been used, but it was desirable, for the proof of concept, to remain perfectly planar to reduce simulation times and simplify the geometry).

For the designs to function as simulated, care must be taken to duplicate the packaging conditions that will be seen by the final filter. Ground boundaries were chosen close to the edges of the filters during planar EM

simulation. Adjustments were then made to the filter elements to compensate for packaging effects. Once completed, the boundary conditions are then mimicked during fabrication by placement of grounded via columns as shown.

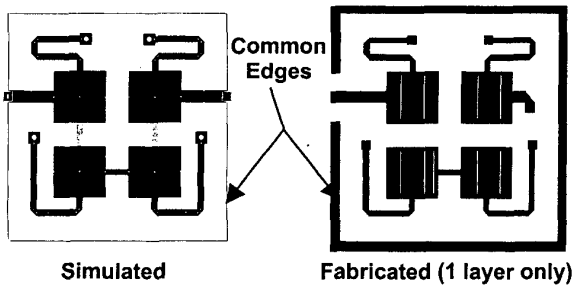

Fig 5. Ground Wall Boundary Mapping

The complete filter section was realized by stacking the low pass filter on top of the high pass filter, with an embedded attenuator (3dB) included between the filters to ensure minimal interaction. Care was taken to ensure the surface component layout and vertical interconnections were compatible with the size and layout of the embedded filters.

Once fabricated, the embedded filter structure was tested and compared for accuracy with simulated results. Simulations for nominal material parameters (height of 7.4 mils, ε_r of 5.9) were slightly high, but measurements showed that the tape layer undergoes a slight compression (the height was 7.0 mils, about 5%) when placed between the parallel plates of the capacitors. It is also reasonable to assume that the material in the compressed region would be denser, leading to a proportional increase in εr as well. The effect would be slightly larger series capacitance than modeled at the nominal thickness and a lower center frequency. Simulations for the compressed parameters (height of 7.0 mils, ε_r of 6.2)seem to bear this out.

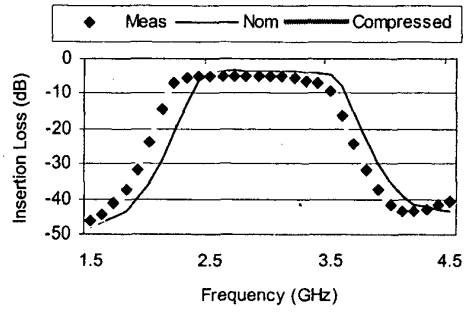

Fig 6. Insertion Loss of Embedded LPF/HPF

Upon inspection, it was noted that the tape spacing between conductor layers was compressed about

III. Frequency Doubler

A summary of the doubler substrate stack is shown below:

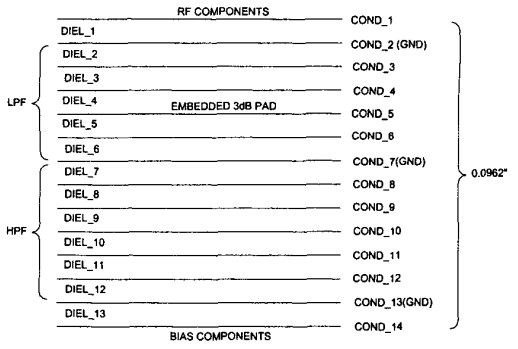

Fig 7. Conductor/Dielectric Layer Structure

The ground layers consist of 10 mil x 10 mil grids (required for layer adhesion), while interconnection between layers and to ground was achieved using 6 mil diameter vias. The substrate was fabricated at Kyocera-Vispro Division in Beaverton, OR. Standard design rules were maintained in the layout. A photo of the stage is shown below:

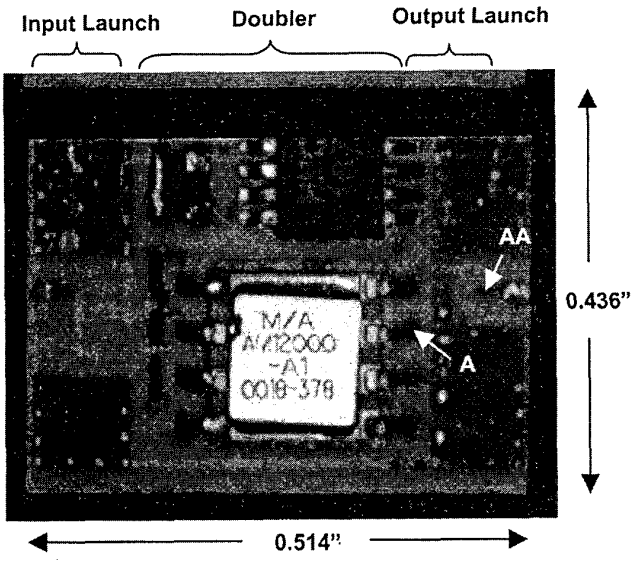

Fig 8. Frequency Doubler Test Circuit

A spectrum analyzer was used to capture the fundamental input (f_o=1250-1750 MHz), the doubled output ($2f_o$) and unwanted leakage (at f_o and $3f_o$).

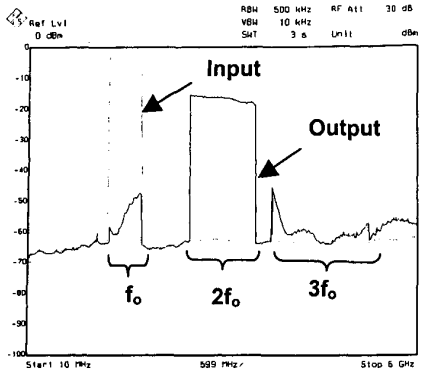

Fig 9. Frequency Doubler Module Spectral Output

The 3rd harmonic leakage is dictated by the embedded filter response (a higher order low pass filter and better design centering is needed). The fundamental frequency leakage is due to direct radiation from the amplifier output to the launch pin (see Fig 8, points A and AA) and is not related to the embedded filter. Isolation measurements of isolation between these points is shown below:

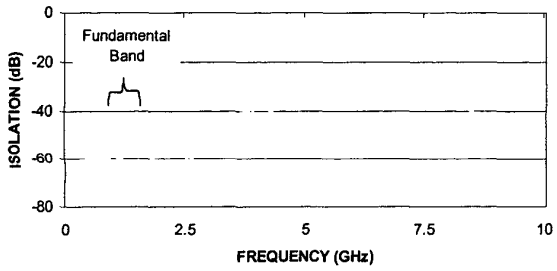

Fig 10. Isolation Between Amplifier and Launch.

Even though via walls were used to isolate these points (internally and on the surface), only about 60 dB of isolation was achieved at the fundamental frequency. Due to conversion and filter losses, the fundamental signal at the amplifier (14 dBm) will be significantly higher than the desired output at the launch (-17 dBm), so that this isolation proves marginally acceptable. The isolation degrades further above 5 GHz, indicating that isolation requirements (especially for switches) may prove to be difficult to meet for high frequency LTCC circuits, and better isolation strategies would be required for high frequency applications. The conversion loss of the multiplier stage was characterized for input frequencies of 1250-1750 MHz (output frequencies of 2500-3500 MHz).

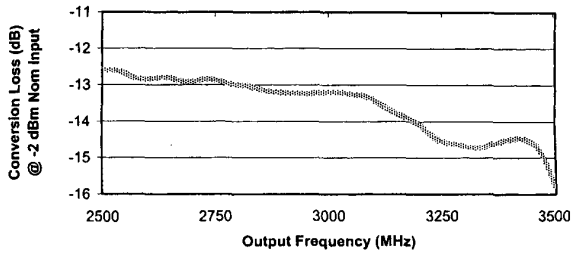

Fig 11. Measured Conversion Loss

The conversion loss drops 3 dB across band with increasing frequency due to a noticeable disturbance at the upper roll-off, which may be attributed to design of the low pass filter section.

IV. Conclusions

We have demonstrated an L-Band frequency doubler in a reduced footprint package using a low temperature co-fired ceramic substrate with embedded filters. Overall, the response of this initial test circuit is encouraging, and the module, as presented, would be usable in our systems. Future work will focus on miniaturization of higher frequency designs as well as advanced packaging concepts for these modules.

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